1992

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TITLE:

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DATE: May 31, 1992

COMPARISON OF SODIUM CONTAMINATION LEVELS IN PLASMA ENHANCED DIELECTRICS USING VARIOUS ETCHBACK, PLANARIZATION, AND POST CLEANING TECHNIQUES

by

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A Thesis

Presented to the Graduate Committee

of Lehigh University

in Candidacy for the Degree of

Master of Science

in

Materials Science and Engineering

Lehigh University

1992

Certificate of Approval

This thesis is accepted and approved in partial fulfillment of the requirements for the degree of Master of Science.

5/15/92

(date)

Professor in Charge

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ACKNOWLEDGEMENTS

The author would like to express her appreciation to her advisor R. Jaccodine, at Lehigh University, along with J. A. Shimer and C. W. Wilkins, at AT&T Bell Laboratories, for their guidance, encouragement and support. In addition, she would like to thank: J. Cassano, H. Chew and E. P. Martin for technical support; and F. T. Herring and L. D. Snyder for reviewing this thesis. In addition, special thanks to J. Swiderski, who provided encouragement and guidance throughout the degree program.

The author expresses her gratitude to her friends and family. Most importantly, to Mark Earl Bollinger, who provided his love and support throughout these years of study. This thesis is dedicated to her mother and two daughters: Christine, Lauren and Meredith.

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Abstract

Multilevel metal interconnects in VLSI circuits require increased planarization for photolithography and for improved metal reliability. New materials and processes are needed to meet these requirements. One process being evaluated is resist etchback (REB) planarization. However, with the introduction of this process into the VLSI technology, a study was necessary to determine if the process introduced higher than normal levels of sodium into the dielectric.

This research compared various dielectric etchback processes including the REB planarization process to quantify the levels of sodium introduced for each process. Comparison of two different post cleaning techniques with films that did not receive wet chemical cleaning was also part of this research.

A separate study was also performed to determine if a phosphorus doped plasma enhanced chemical vapor deposition (CVD) dielectric could getter the sodium introduced by a particular etch back process.

The triangular voltage sweep (TVS) method was chosen to quantify the amounts of sodium introduced by each etchback process.

The results indicate that the REB planarization process introduces an extremely high level of sodium (8E13 cm^{-2}). The post cleaning results show that the 100:1 hydrofluoric acid is more effective in removing the sodium contaminated layer of dielectric than the ethylene glycol/buffered hydrofluoric etch.

In addition, this study shows that a low temperature phosphorus doped plasma enhanced CVD dielectric is capable of gettering the sodium incorporated into the dielectric during oxygen plasma photoresist stripping.

In conclusion, introducing a new etch process, such as REB planarization, into a multilevel metal interconnect technology, requires a complete evaluation of the process for sodium contamination. Using the TVS method, quantitative information can be obtained and the specific step in the process sequence that is responsible for the contamination can be determined.

1. Background

1.1 Purpose

A multilevel interconnect structure includes a series of dielectric and metal levels. The process discussed here will be a three metal technology as shown in figure 1.

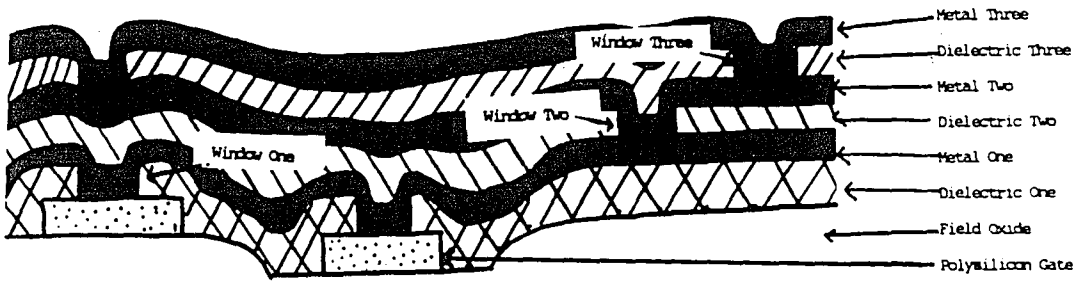

Figure 1. Three Level Metal Technology

Certain steps in state-of-the-art CMOS (complementary metal oxide semiconductor) processing introduce mobile ions which form a thin layer of contamination at dielectric surfaces as shown in figure 2.

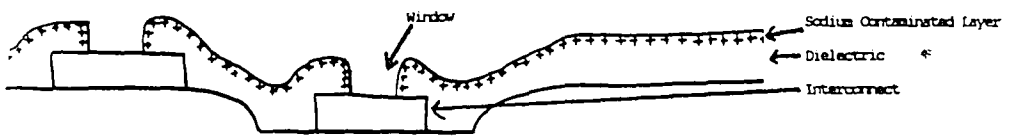

Figure 2. Contaminated Sodium Layer Introduced Into Undoped Dielectric

In undoped dielectrics, if this layer is not removed with a wet chemical clean, mobile ions present in the dielectric can degrade the circuit's performance by causing long term drift in transistor threshold voltage.[1]

1.2 Mobile Ion Contamination

Stripping photoresist in an oxygen plasma introduces sodium into the dielectric.[2] [3] In addition, some reactive ion etch (RIE) processes[4] introduce mobile ions into the dielectric film by operator handling and by buildup of sodium deposited on the reactor walls during the RIE process in the presence of photoresist. With use, the mobile ion concentration of the reactor will continue to increase unless proper cleaning procedures for the reactor are followed.

In this work, the RIE process used to etch the oxide combined with the process of etching photoresist introduces very high levels of mobile ion concentration.

1.3 Ionic Mobility

Not all sodium that is incorporated in the dielectric film becomes mobile.[5] Some of the sodium is bound in the lattice, and therefore the sodium is electrically inactive and remains unchanged and immobile. Different oxide growth conditions and deposition techniques can affect the amount of inactive sodium.[6] ,[7] M. W. Hillen and J. F. Verwey[6] show the influence of oxide growth conditions on the mobility of sodium as shown in Table 1.

Oxide Growth Ambient Temperature (°C)	μ_0 ($cm^2v^{-1}s^{-1}$)	E_d (eV)
dry O_2, 1200	40	0.70
steam, 1150	3-12	0.62
dry O_2, 1150	0.46	0.63
dry O_2, 1100	1.0	0.66
O_2/HCl, 1150	1.0	0.66

TABLE 1. Drift mobilities of Na^+ ions in SiO_2.[6]

Sodium ions after drifting to the interface can be viewed as a sheet of charge. D. J. DiMaria[8] found that this sheet of charge is within fifty angstroms of the interface.

A very important observation is that the same number of sodium ions can be cycled back and forth through the oxide between the silicon and metal electrode several times. Sodium ions do not exchange charge with either electrode and do not become discharged when they build up to within tunneling distances of the electrode. It is the failure of the sodium to discharge accompanied by the high mobility in the oxide film that causes instability in silicon devices.

The structure discussed here is a MOS capacitor (figure 3) formed by depositing a dielectric film on a silicon substrate followed by the deposition of a metal or metal alloy. The metal is then patterned and etched to provide the top plate of the capacitor.

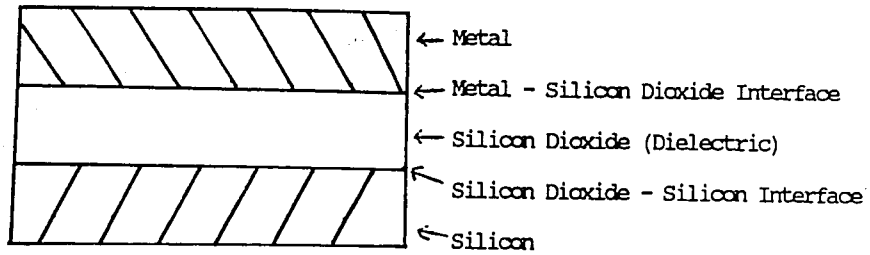

Figure 3. MOS Capacitor

S. R. Hofstein[9] has proposed that sodium ions are trapped in potential wells near the silicon-silicon dioxide and the silicon dioxide-metal interfaces and an ionic current is only produced when the sodium ions are thermally excited out of these wells. Ion traps are associated with structural defects in the interfacial layers (i.e., the transition regions between the silicon or metal lattice and the silicon dioxide).

Sodium moves through the silicon dioxide by interstitial diffusion as shown in figure 4.

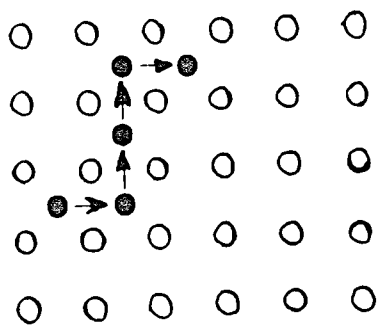

Figure 4. Interstitial Diffusion By Jumping.[10]

In this direct mechanism, the sodium ion does not have a strong bonding interaction with the silicon dioxide lattice and jumps between the interstices. Figure 5 illustrates how the sodium will drift through the silicon dioxide under the influence of an electric field.

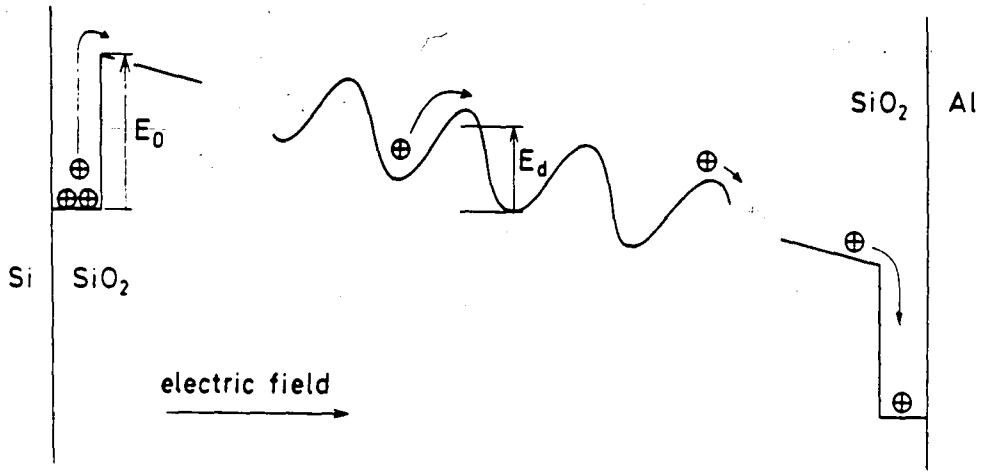

Figure 5. Model of Ion Transport In Dielectric Layer[6]

To understand ion motion, assume that all the ions are initially trapped near the silicon-silicon dioxide interface. The sodium ions escape from the traps when thermal energy is applied by increasing the temperature of the sample.

Under the influence of an electric field, the sodium ions begin to drift to the silicon dioxide-metal interface where they are bound in ion traps. The direction of ionic motion can be changed by reversing the applied voltage, as was shown by Nicollian and Brews.[1]

When a dielectric is contaminated with sodium which is mobile under the influence of electric field at elevated temperatures, these mobile ions contribute an additional component to the displacement current. This ionic component can be analyzed to quantify the amount of sodium present and may provide some additional information on sodium's transport properties. This will be shown in the following analysis.

The MOS capacitor with a space charge density of $\rho(x)$ in the dielectric is shown in the energy band diagram in figure 6.

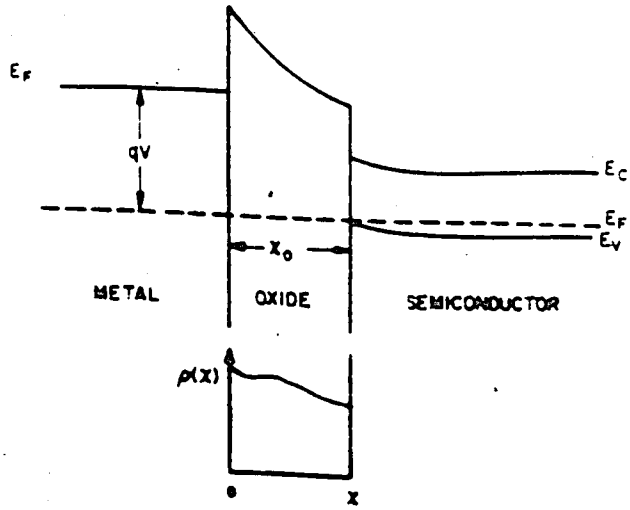

Figure 6. Electron Energy Diagram of a MOS Structure in Accumulation. The banding bending is characteristic of a P-type semiconductor.

The total charge induced in the silicon substrate near the dielectric interface when a voltage V is applied to the metal field plate is given by

$$Q(v) = -\int_0^v C(v)\,dv + C_i\phi_{ms} - \int_0^{x_i} \frac{x}{x_i}\rho(x)\,dx \tag{1}$$

where $\rho(x)$ is the charge distribution in the oxide, C_i is the dielectric capacitance, ϕ_{ms} is the metal-silicon work function, x_i is the dielectric thickness, and C(V) is the total MOS capacitance.

As the voltage varies, the current is

$$I = \frac{-dQ(v)}{dt} = \frac{d}{dt}\int_0^v C(v)\,dv + \frac{d}{dt}\int_0^{x_i} \frac{x}{x_i}\rho(x_i,t)\,dx. \tag{2}$$

If the voltage varies linearly, $V = +/\alpha t$, and (2) becomes

$$I = \pm\,\alpha C(v) \pm \alpha\frac{d}{dV}\int_o^{x_i} \frac{x}{x_i}\rho(x_i,V)\,dx \tag{3}$$

where α is the constant voltage sweep rate.

In equations (2) and (3), the first expression on the right hand side represents the current response of the MOS capacitor. This leads to a quasi-static curve which is used in conjunction with a high frequency C-V curve, to determine interface-trap densities at room temperature. The second expression on the right hand side is the current response associated with the motion of charge in the dielectric as the voltage is changed.

Any contribution of fixed charge will not appear in equation (3) but it would appear in equation (1). The assumption is made that the remaining charge distribution $\rho(x,V)$ can equilibrate with the varying externally applied voltage.

The ramp is varied linearly over a voltage range $-V_o$ to $+V_o$. Integrating equation (3),

$$\int_{-V_o}^{V_o} [I(V) - \alpha\, C(V)]\, dV = \alpha \int_0^{x_i} \frac{x}{x_i} \rho(x,+V_0)\, dx - \alpha \int_0^{x_i} \frac{x}{x_i} \rho(x,-V_0)\, dx. \qquad (4)$$

With a large positive voltage on the metal field plate, the positive charge will drift to the semiconductor interface and vice versa. Approximating the charge distribution at the extreme voltages by delta functions, using the integral properties,

$$\int_{-V_o}^{V_o} [I(V) - C(V)]\, dV = \alpha \int_o^x \frac{x}{x_i} \rho\delta(x-x_i)\, dx - \alpha \int_o^{x_i} \rho\delta(x)\, dx = \alpha\rho_i \equiv \alpha Q_m \equiv \alpha_q N_m \qquad (5)$$

Therefore, a current versus voltage measurement will yield the mobile-ion content, N_m, if the integral $\int_{-V_o}^{V_o} I(V)dv$ can be evaluated, α is independent of time and is known, and the quantity $\alpha \int_{-V_0}^{V_o} C(V)dV$ can be determined.

1.4 Detection and Measurement of Sodium

There are two techniques which have been used for over twenty years to detect mobile ions. Triangular voltage sweep (TVS) and capacitance-voltage (C-V) are reliable techniques to detect mobile ions in films. However, there are clear advantages for selecting the TVS technique rather than the C-V technique. These advantages have been documented by Nicollian and Brews[1] and include:

1) the mobile ion density is obtainable even when the interface trap level density changes or if there is gross nonuniformity in interfacial charge.

2) different mobile ion species can be identified from one another.

3) the TVS technique is able to detect densities as low as 1E9 cm^{-2}.

4) TVS measurements tend to be faster because only one measurement is necessary to obtain the concentration and species of the mobile ions.

Physical methods such as neutron activation analysis, flame photometry and secondary ion spectroscopy can be used to determine the total mobile ion concentration but these methods are destructive and time-consuming.

M.Yamin[11] was the first to utilize the TVS technique to evaluate the charge effect on silicon dioxide films. He pointed out that there are three voltage regions when using the TVS technique:

1) a region of non-conduction at the positive silicon voltage.

2) a region of charge storage and discharge in which the sample has increased differential capacity.

3) a region of "ohmic" conduction in the negative side of the charge-discharge region.

In the TVS method, the capacitor is held at a constant elevated temperature and a linear voltage ramp is applied to the bottom substrate bias as the mobile ions drift from one electrode to the other. The triangular ramp voltage sweeps the ions to the other electrode and the measured current changes direction.

M. Kuhn and D. J. Silversmith[12] used the TVS technique and studied in more detail the effect from mobile ion contamination. They reported that the ionic displacement in an MOS capacitor could be measured performing the test at elevated temperatures.

Kuhn and Silversmith noted that the slope of the ionic displacement current indicated that ionic trapping occurs at both the metal-oxide and silicon-oxide interface. This agrees with the previously mentioned theory proposed by Hofstein.

It was determined that when the oxide contains mobile ions which move under an electric field at elevated temperature, the mobile ions contribute to the displacement current.[12] With this information, the concentration as well as the transport properties can be determined.

At room temperature the current is proportional to the low frequency differential capacitance of the material as shown in figure 7 (Curve A). Increasing the temperature, increases C_{min}/C_{ox}, which is the ratio of the smallest to the largest capacitance as a function of oxide thickness. At a temperature of 300 °C, the current of an uncontaminated device becomes almost equal to C_{ox} as shown in figure 7 (Curve B). When mobile ions are present, a current peak near $V_G=0$ is superimposed on the curve illustrated in figure 7 (Curve C). At large negative bias, all the mobile ions are at the metal electrode-oxide interface and the current that flows is proportional to C_{ox}. As the voltage increases, the mobile ions begin to move toward the silicon-oxide interface, attracting a large number of electrons to the silicon surface. As the mobile ions are moving, additional electrons flow from the metal to the silicon through the external circuit. The current increases with the increased flow of

electrons. A peak in the current is detected when a large number of mobile ions are moving through the oxide. Continuing to increase the voltage, there are fewer ions flowing, and the increased current drops. The current becomes proportional to C_{ox} after all the mobile ions have drifted to the interface at the given temperature.

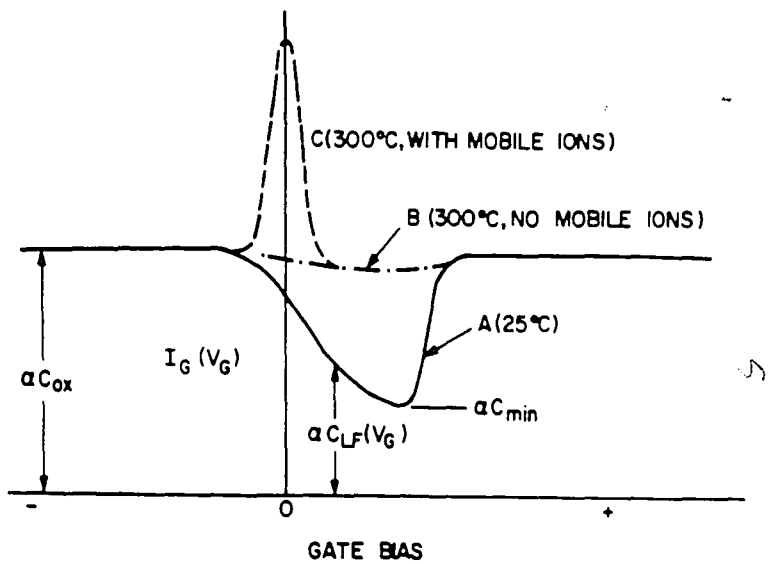

Figure 7. Current as a function of bias in response to a linear voltage ramp in a MOS capacitor having a P-type substrate.

1.5 Gettering of Sodium Using Phosphorus

A phosphorus doped dielectric getters the sodium ion effectively.[13] The phosphorus immobilizes the sodium ions within the dielectric layer, preventing their drift under bias and temperature. In past work, a high temperature (> 800 °C) was thought to be necessary in gettering the sodium.

2. Experimental

2.1 Description of Multilevel Metal Interconnect Process

As mentioned earlier the process discussed here will be a three level metal technology as shown in figure 1.

In this process, dielectric 1 is deposited after the formation of the transistors. Dielectric 1 is deposited using a chemical vapor deposition (CVD)[14] technique with a thin undoped layer (≈ 2000Å) followed by a doped layer (≈ 3000Å). The undoped layer is deposited to prevent autodoping in the source/drain regions of the transistors. The second layer is doped with phosphorus or a combination of phosphorus and boron. The phosphorus getters any mobile ions introduced during processing and boron improves the flow characteristics of the dielectric in the subsequent high temperature furnace step. After dielectric 1 is deposited and flowed, the process continues with a photolithography step and window contact etch. Contacts are formed by depositing a metal (Aluminum) or metal alloy (Aluminum-Silicon) using physical vapor deposition (PVD)[15]

Metal 1 is patterned and etched to provide the first metal interconnect of the circuit. The metal 1 level has a eutectic temperature of ≈ 550 °C, placing a constraint on the temperature in subsequent processing steps. A second dielectric is deposited after metal 1 and several techniques can be used at this stage of the process. It is important in the integration of a multilevel interconnect process to smooth the dielectric to provide a surface that will promote acceptable metal continuity and good interlevel isolation.

The process commonly used for dielectric 2 uses a plasma enhanced CVD technique with tetranethylorthosilicate (TEOS) as the source gas.[14] The deposition temperature is ≈ 390 °C and the film as deposited is referred to as "PETEOS". The dielectric 2 thickness of

≈ 10,000 Å is necessary to provide sufficient isolation between metal 1 and metal 2 interconnect levels. However, as geometries decrease and as the metal 1 interconnect runners are placed closer and closer together, a single deposition of PETEOS frequently results in the formation of voids and cusps as shown in figure 7.[16]

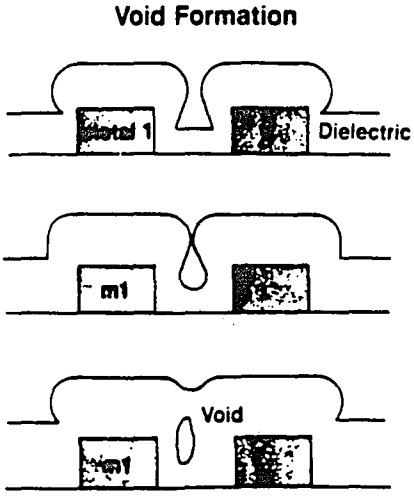

Figure 8. Void Formation in Closely Spaced Interconnect Runners.[16]

A modification to the process is necessary and includes a thinner PETEOS deposition (<10,000 Å) followed by a reactive ion etchback (<6,000 Å) to provide a means to fill the gap between closely spaced runners.[17] The dielectric process is completed by depositing a second layer of PETEOS to meet the thickness requirements of 10,000 Å. The topography of this dielectric is still quite rough, however, and a second modification to the dielectric process can be made by depositing a thick second layer (>20,000 Å) and performing an additional reactive ion etchback to achieve a smoother topography.[17]

The non-planarized approach is as follows:

1) Process wafers to and including metal 1 etch
2) Deposit PETEOS
3) Etchback PETEOS *
4) Deposit PETEOS
5) Etchback PETEOS *
6) Apply photoresist and print vias
7) Reactive ion etch vias *
8) Oxygen plasma photoresist strip *
9) Deposit metal 2, pattern and reactive ion etch

Wafers processed through the above steps will have mobile ion content of greater than 1E13 cm^{-2} on the surface. The addition of a wet chemical clean after steps 3, 5, 7, and 8 removes the thin layer of contaminated dielectric and reduces the mobile ion content significantly (<5E11 cm^{-2}). The wet chemical clean conditions are tailored to the surface depth of the contamination.

A planarized dielectric surface can be achieved using a Resist EtchBack (REB) planarization process.[16] In this process, a thin deposition of PETEOS is followed by a reactive ion etchback (identical to the process discussed earlier) and a thick PETEOS layer ($\approx$ 20,000 Å) is deposited. Instead of performing a reactive ion etchback at this step, photoresist is applied. The etchback of the dielectric 2 is performed using an etch process which etches; 1) photoresist alone; 2) photoresist and PETEOS at the same rate; 3) PETEOS alone. This etchback technique provides a planar surface for the metal 2 which will improve continuity and isolation.

After the REB planarization step has been completed, vias are patterned and etched to provide contact from metal 2 to metal 1. Metal 2 is deposited, patterned and etched using the same process as metal 1 to provide the second metal interconnect. Dielectric 3 and metal 3 interconnect use the same process steps as dielectric 2 and metal 2 interconnect, respectively.

The planarized approach is as follows:

1) Process wafer to and including metal 1 etch
2) Deposit PETEOS
3) Etchback PETEOS *
4) Deposit PETEOS
5) Apply photoresist
6) Planarization Etchback *
7) Apply photoresist and print vias
8) Reactive ion etch vias *
9) Oxygen plasma photoresist strip *
10) Deposit metal 2, pattern and reactive ion etch

Following the REB planarization process requires a longer wet chemical clean due to the increased mobile ion content. The increase can be explained by the physical removal of the photoresist using a reactive oxygen chemistry during the first etch step in the REB process thus providing an elevated level of sodium in the reactor which is driven deeper into the oxide due to enhanced ion bombardment.

2.2 Design of Experiments

Measurements were made using the TVS technique described earlier. The first experiment includes a set of five main groups, each containing three subgroups.

The results from the first experiment provided information about the cleaning steps required to insure a mobile ion free dielectric.

In the second experiment, phosphorus doped PETEOS was evaluated for its effectiveness in gettering sodium at temperatures below 400 °C.

2.2.1 Mobile Ion Concentration in Various Processes

This experiment included reactive ion etching in a hexode reactor (exsitu etchback) and a single wafer reactor (insitu etchback). The resist etchback planarization process was

compared to the standard etchback process.

In addition, two different wet chemical clean procedures were compared with films that did not receive wet chemical cleaning.

After groups (1) to (5) were processed, one third of the wafers were (a) not etched and would act as the control group; (b) etched in 8:1 ethylene glycol/buffered hydrofluoric acid for 0.8 minutes; and (c) etched in 100:1 hydrofluoric acid for 3 minutes. Process flow charts for each group are shown in figures 9-13.

The outline of the experiment is shown below:

1) As Deposited Film	a) No Clean b) 0.8 minutes EG/BHF c) 3 minutes 100:1 HF
2) Deposit PETEOS Exsitu Etchback in Hexode Reactor 1.0 minute Ethylene Glycol/BHF Deposit PETEOS	a) No Clean b) 0.8 minutes EG/BHF c) 3 minutes 100:1 HF
3) Deposit PETEOS Apply Photoresist Oxygen Plasma Photoresist Strip	a) No Clean b) 0.8 minutes EG/BHF c) 3 minutes 100:1 HF
4) Deposit PETEOS Insitu Etchback in Single Wafer Reactor Deposit PETEOS	a) No Clean b) 0.8 minutes EG/BHF c) 3 minutes 100:1 HF
5) Deposit PETEOS Apply Photoresist Planarization Etch in Hexode PRS1000 Photoresist Strip	a) No Clean b) 0.8 minutes EG/BHF c) 3 minutes 100:1 HF

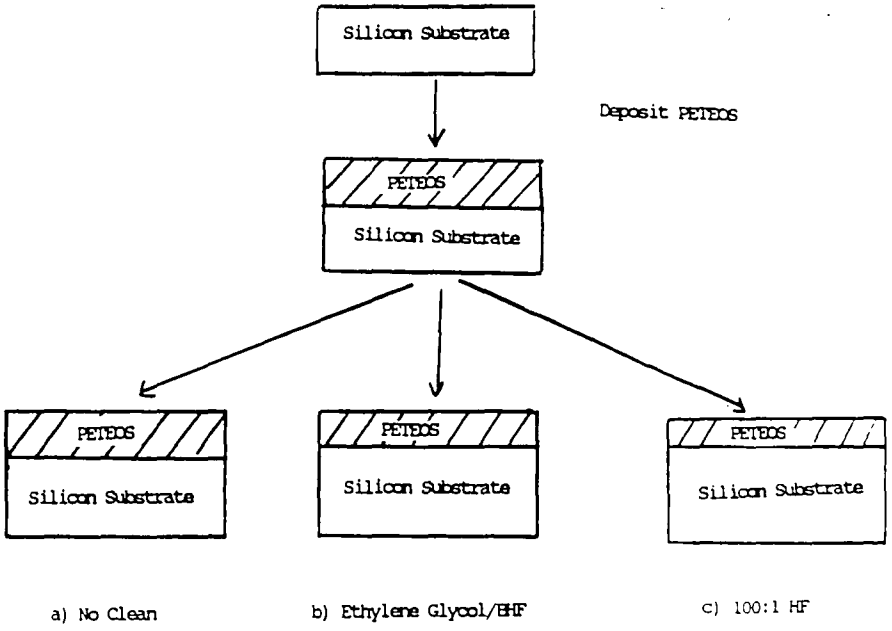

Figure 9. Flow Chart for Group 1 Process Sequence.

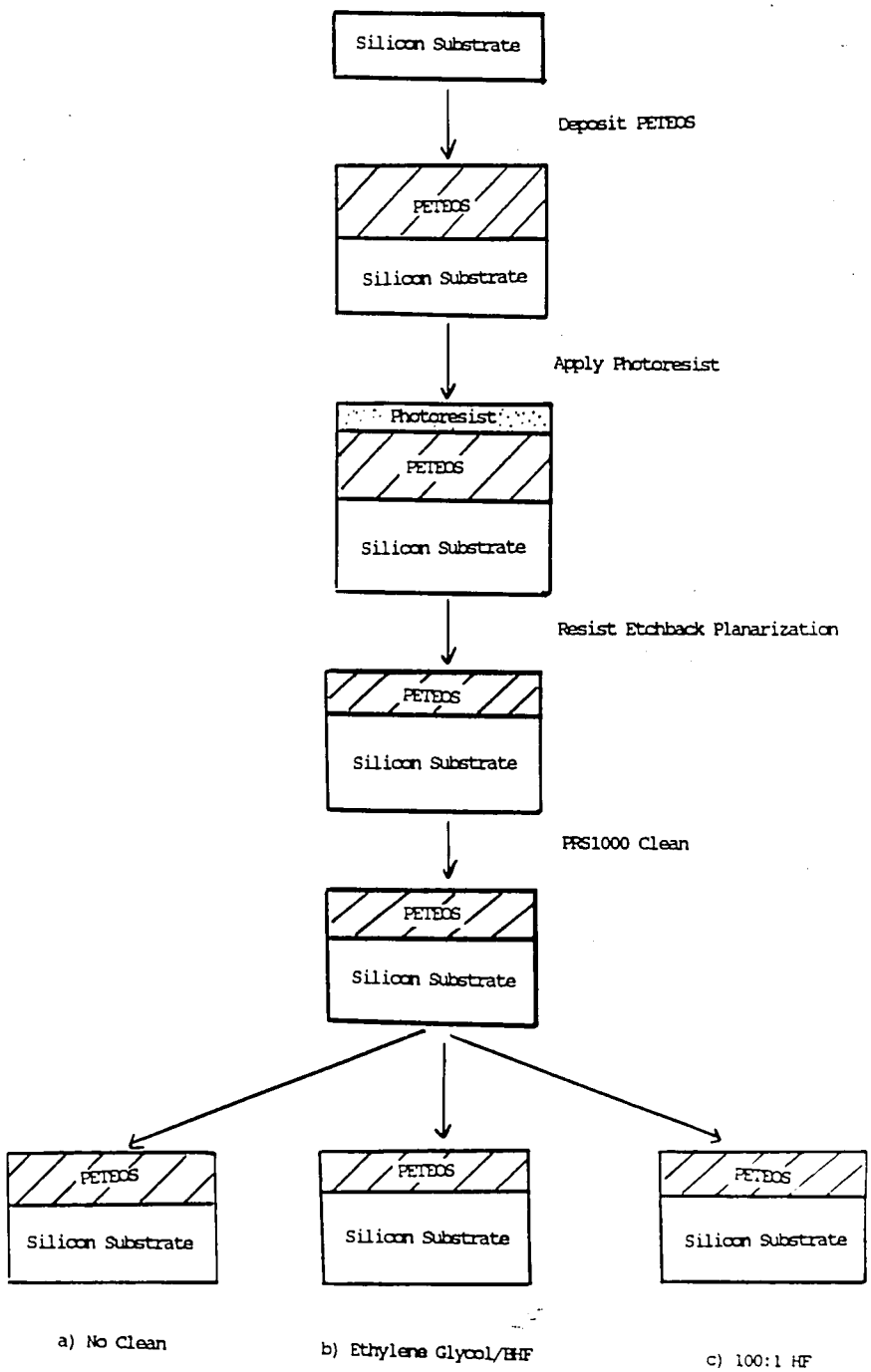

Figure 10. Flow Chart for Group 2 Process Sequence.

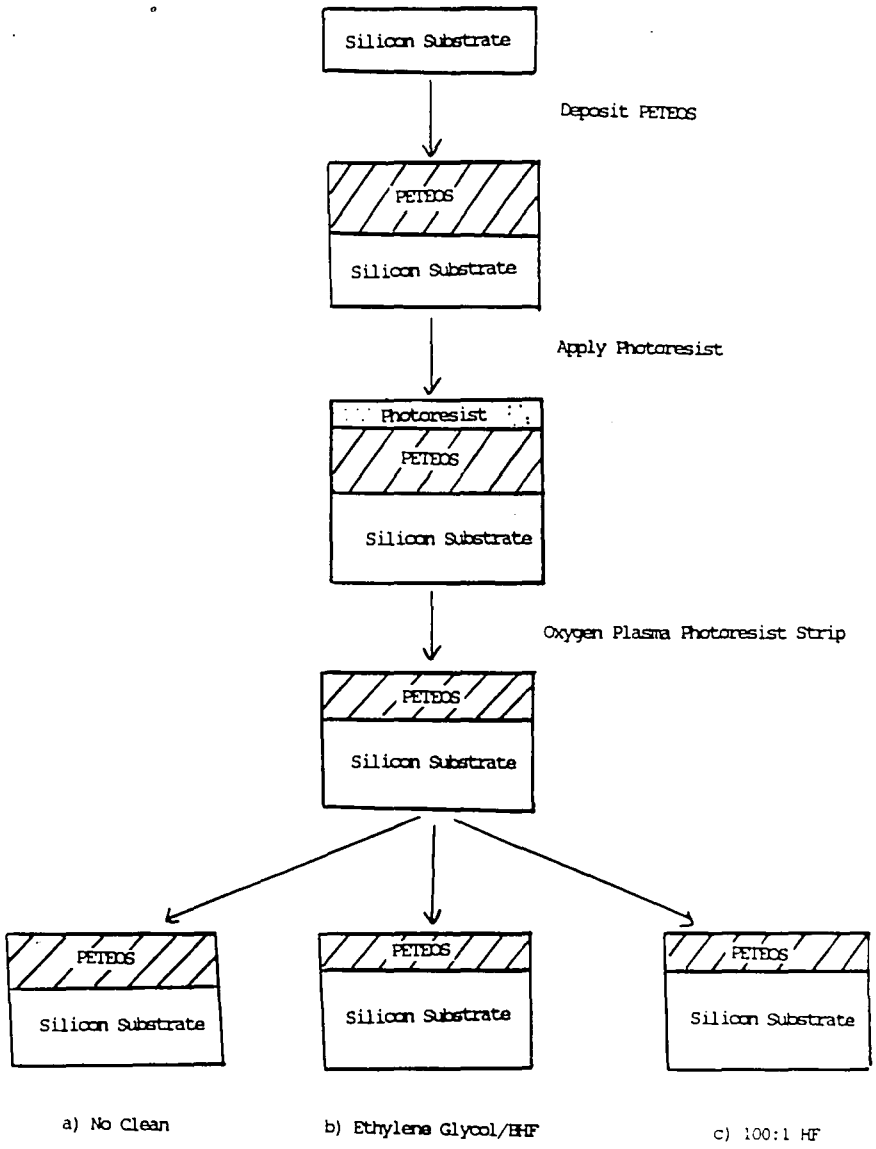

Figure 11. Flow Chart for Group 3 Process Sequence.

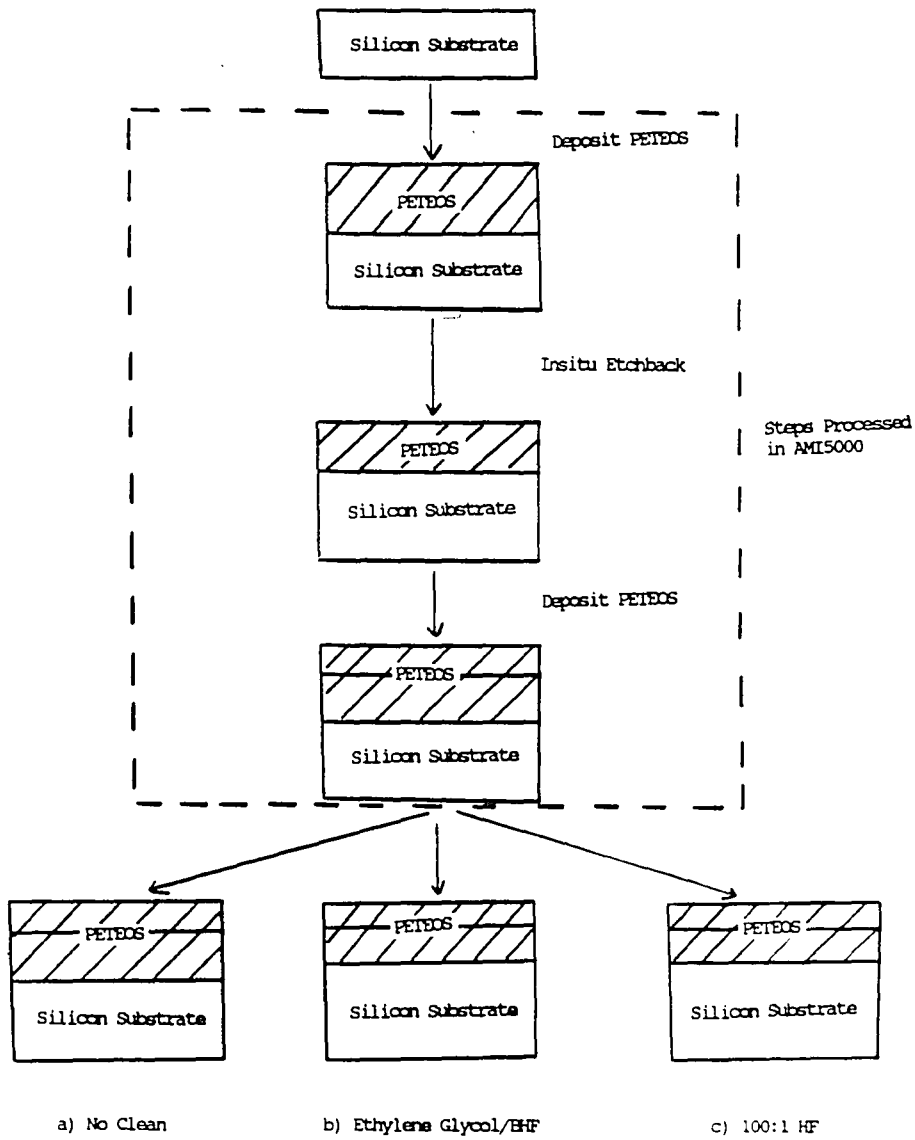

Figure 12. Flow Chart for Group 4 Process Sequence.

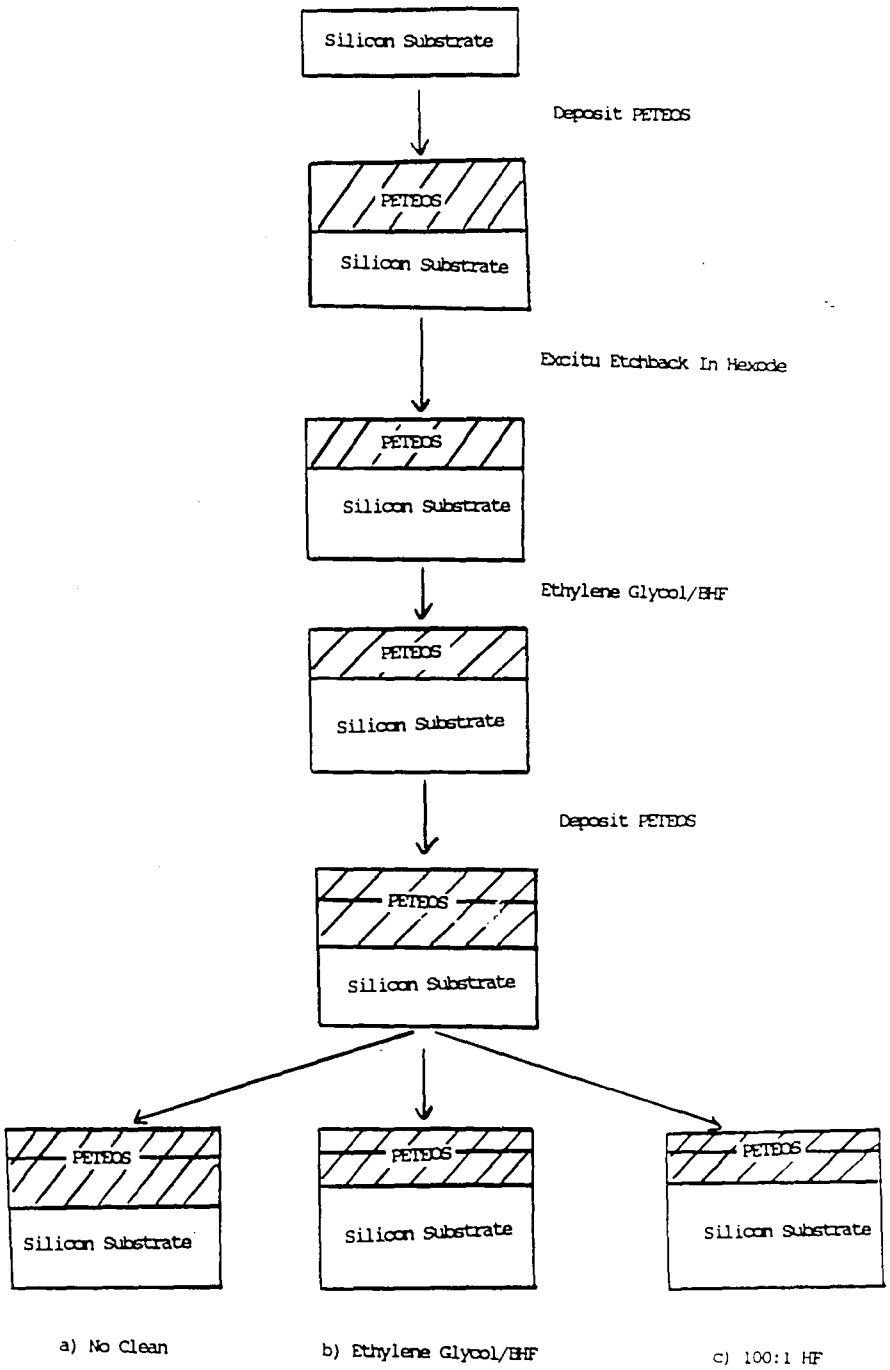

Figure 13. Flow Chart for Group 5 Process Sequence.

Subgroup 1a is important as a control to guarantee that the starting material prior to any processing was not contaminated before the subsequent processing steps. Subgroups 1b and 1c are included to detect any contamination from the wet cleans alone. A contaminated etch bath could increase the mobile ion concentration. Groups 2 and 4 compare the exsitu etchback process in the hexode batch reactor and the insitu etchback process in the single wafer etch chamber. In the process for group 2, wafers were taken from the dielectric deposition tool and etched in a hexode reactor and then taken back to the Applied Materials Incorporated (AMI) 5000 for the second layer of dielectric. Group 4 wafers were kept in the AMI 5000 multichamber system and immediately after dielectric deposition, the wafers went into the insitu etchback chamber for the reactive ion etchback process. After the insitu etchback step, the wafers were transferred into the deposition chamber without leaving the system for the second layer of dielectric. Note that group 2 wafers receive a clean after the first etchback and prior to the second deposition, whereas group 4 wafers do not have any wet cleaning prior to the second deposition of PETEOS. Group 3 provides information on the level of sodium introduced by the removal of photoresist using a reactive oxygen plasma. This step, has been reported in the literature, and is a major source for introducing mobile ion contamination. Group 5 duplicates the REB process used in development of the multilevel interconnect process for a three level metal technology and which was presented in section 2.1.

After each group was processed, a metal alloy was deposited using PVD, printed using a GCA G-line stepper and etched to provide the top plate of the capacitor.

2.2.2 Gettering of Mobile Ions Using Phosphorus

To understand if sodium could be gettered at dielectric 2 using a phosphorus doped PETEOS[18] a second experiment was performed. Group three (PETEOS deposition, apply

resist and photoresist strip using oxygen plasma), was chosen to study the effect of gettering sodium using a doped low temperature PETEOS dielectric. The sodium level obtained for this cell in the first experiment with no cleans was 8E11 cm^{-2}.

The outline of the experiment is shown below:

A) As Deposited PETEOS - No Phosphorus Doping

B) As Deposited PETEOS - With Phosphorus Doping

C) Deposit PETEOS - No Phosphorus Doping
Apply Photoresist
Oxygen Plasma Photoresist Strip

D) Deposit PETEOS - With Phosphorus Doping
Apply Photoresist
Oxygen Plasma Photoresist Strip

Group A is important to insure that the material is clean prior to subsequent processing. Group B provides information on the behavior of the doped dielectric without the presence of sodium. Group C insures that the process does induce high levels of sodium and provides a quantitative number for the amount of sodium contamination in an undoped film. Group D insures that high levels of sodium can be gettered by a low temperature (< 390 °C) phosphorus doped PETEOS film.

2.3 Test Set-Up and Structures Used for TVS Measurements

The TVS system used in this work is shown in figure 14.

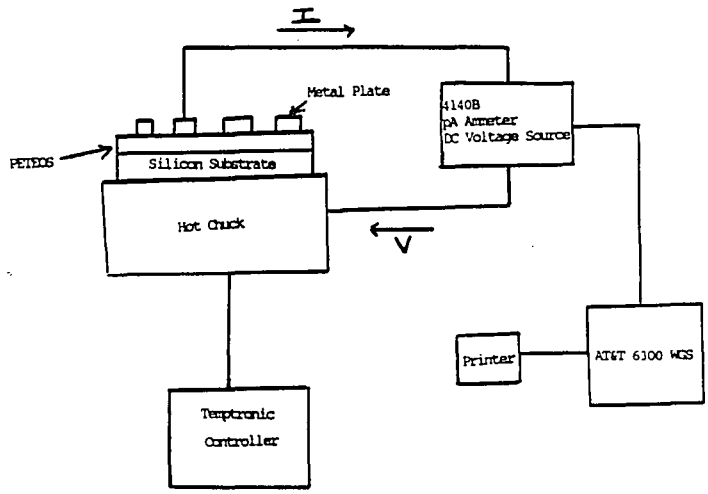

Figure 14. TVS System Used to Detect and Measure Sodium Contamination.

The equipment consists of a shielded probe set with an electrically isolated Temptronic hot chuck capable of temperatures up to 290 °C. The hot chuck is driven with a slow linear voltage ramp supplied by a Hewlett-Packard 4140B (DC voltage source). The displacement current flowing through the capacitor on the wafer chuck is monitored through the probe tip and is measured using the Hewlett-Packard 4140B (pA Ammeter). The output from the ammeter is recorded on an Epson FX-850 printer. An AT&T 6300 WGS using BASIC is used to interface the test equipment with the programs necessary to run the test and plot the resulting TVS trace.

The starting material used was boron doped silicon substrate 125mm in diameter. After the dielectric was deposited on the silicon substrate and each set of process steps was completed, a metal alloy was deposited using PVD. The wafers were patterned using a reticle which included several capacitor sizes. The capacitor tested was 6.4×10^{-2} cm^2 and is

identified in figure 15.

All the tests were run at 290 °C using a sweep rate of 0.5 volts per second.

The sweep rate was chosen to maintain quasistatic equilibrium in the capacitor during the entire measurement.[19] To guarantee that quasi equilibrium is reached during measurement, a second trace was made under the same conditions except for the sweep rate. If the sweep rate is too fast, the sodium ions cannot follow the charge in applied field which will affect the concentration.

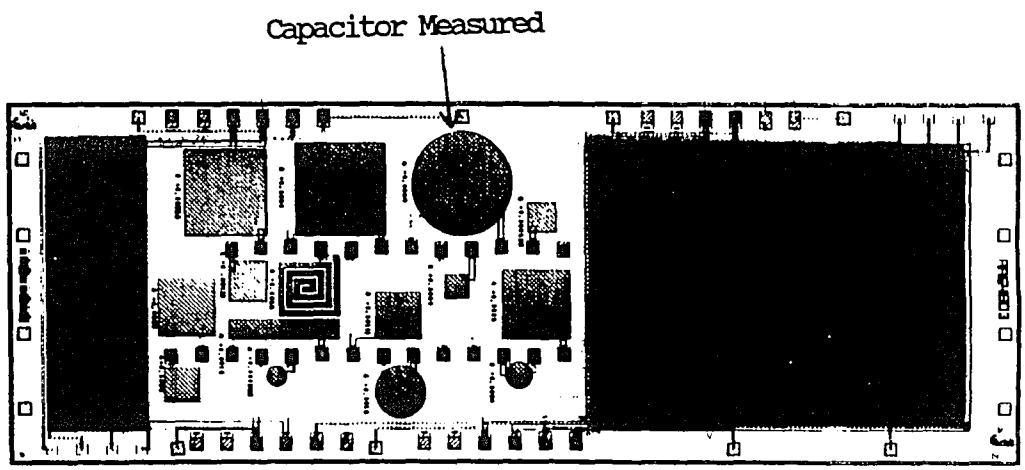

Figure 15. Reticle used to pattern metal alloy. The capacitor tested was 6.4 x 10^{-2} cm^2 and is identified.

3. Results and Discussion

3.1 Mobile Ion Concentration

The results from the first experiment are summarized in Table 2.

Group	No Clean (a)	EG/BHF (b)	100:1 HF (c)
1	none	-9.1E10	0
2	-1.5E11	+5.0E10 -9.3E10	none
3	+8.6E11 -8.7E11	+5.7E10 -1.3E11	none
4	+9.1E10 -2.8E11	+2.6E11 -4.1E11	+2.4E11 -3.9E11
5	+8.3E13 -9.4E13	+3.0E13 -2.4E13	+5.0E10 -2.4E11

TABLE 2. Sodium concentration Detected Using TVS Measurement Method.

The control subgroup, 1a, in figure 16a shows that no sodium is present in the as deposited film prior to processing. Subgroup 1c in figure 16c also shows no presence of mobile ions, however, subgroup 1b in figure 16b shows a unimodal peak after the ethylene glycol/buffered hydrofluoric etch. It appears that the EG/BHF etch introduces a low level of sodium into the film. This is a static bath and is changed on a biweekly basis. The sodium level in the bath may actually increase with use and cause some slight amount of contamination. The 100:1 hydrofluoric etch is a recirculating bath and may explain why this etch does not introduce the level of sodium that EG/BHF does.

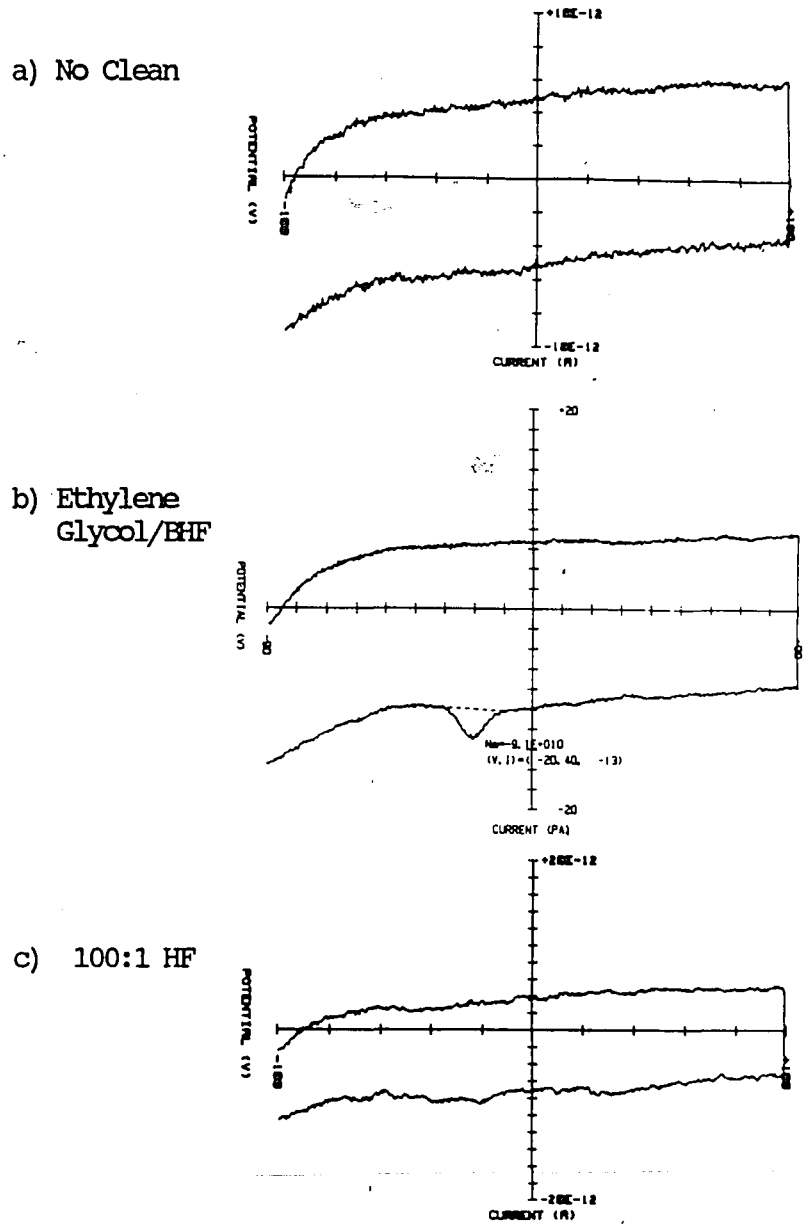

Figure 16. TVS Traces Obtained for Group 1.

Wafers processed in group 2 received the etchback in the hexode, followed by a wet chemical clean prior to the second dielectric deposition. All three subgroups are found to have a low level of sodium, but the wet chemical clean after the second deposition appears to have little effect on the sodium concentration. TVS traces for Group 2 are shown in figure

17a, 17b, and 17c.

a) No Clean

b) Ethylene Glycol/BHF

c) 100:1 HF

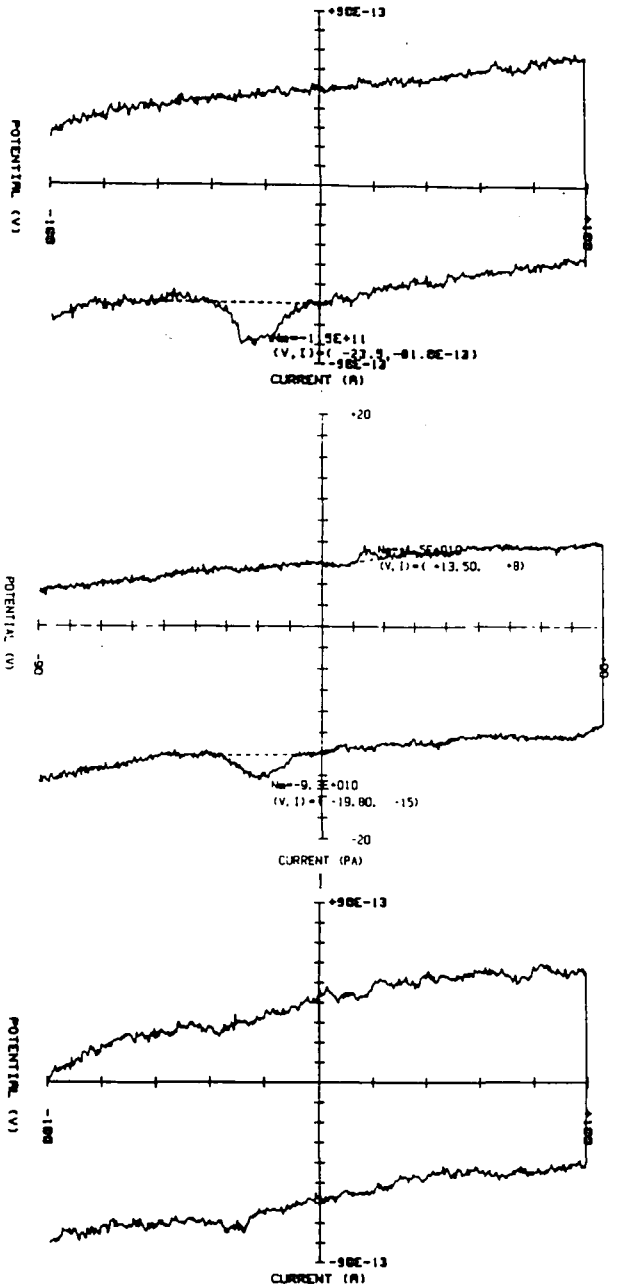

Figure 17. TVS Traces Obtained for Group 2.

Wafers from subgroup 3a in figure 18a were the key to understanding the level of contamination due to the oxygen plasma photoresist strip. Without any wet chemical cleans, the sodium content was ≈ 8.3E11 cm^{-2}. Subgroups 3b (in figure 18b) and 3c (in figure 18c)

showed decreased levels of sodium, with subgroup 3c having no trace of mobile ion contamination. The EG/BHF etch removes some of the contaminated dielectric film but does not remove all of the sodium. The 100:1 HF etch appears to remove all of the contaminated dielectric from the film.

a) No Clean

b) Ethylene Glycol/BHF

c) 100:1 HF

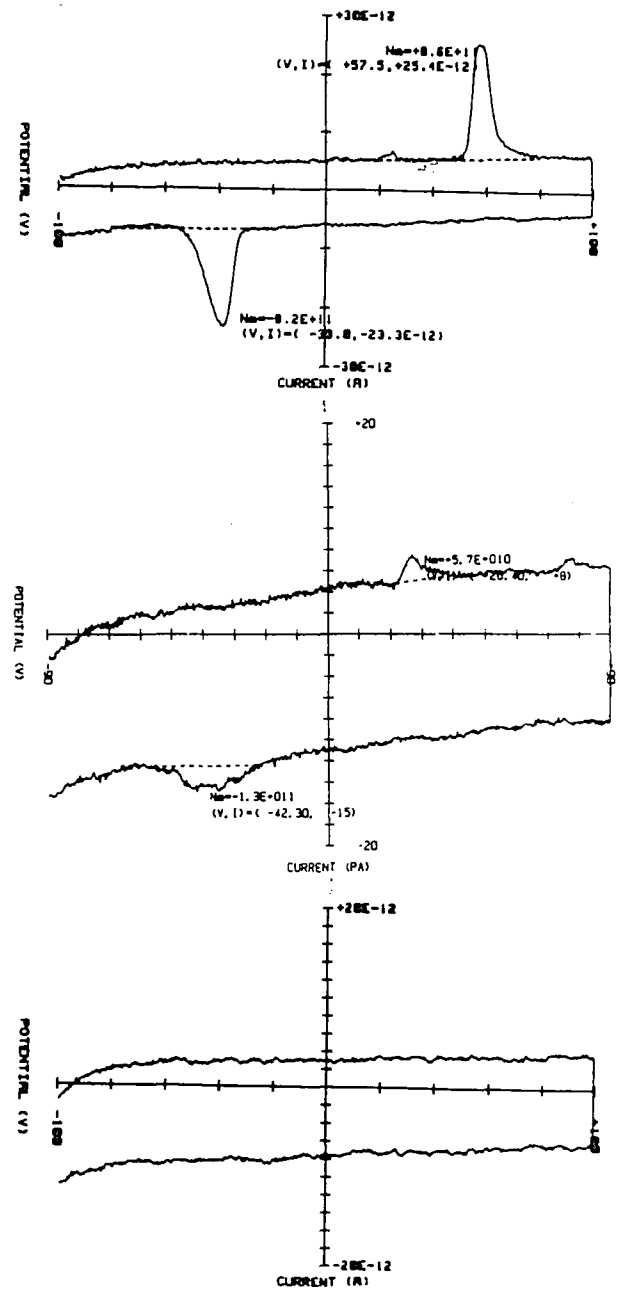

Figure 18. TVS Traces Obtained for Group 3.

Group 4 wafers were processed in the AMI 5000 multichamber received a wet chemical clean only after the second dielectric deposition. All three subgroups had sodium levels of ≈ $3E11cm^{-2}$. These results indicate that the insitu process can induce unacceptable levels of sodium. For this reason, integration of the insitu process must be well characterized. The sodium detected in these films was introduced during the insitu etchback step and the wet chemical clean after the second deposition will have no effect as is shown by the high levels of sodium. A clean is necessary after the first etchback of the dielectric and before the second deposition, as was performed in the exsitu process. These results raise the question as to the possibility of an insitu process including deposition and etchback. TVS traces for Group 4 are shown in figure 19a, 19b, and 19c.

a) No Clean

b) Ethylene Glycol/BHF

c) 100:1 HF

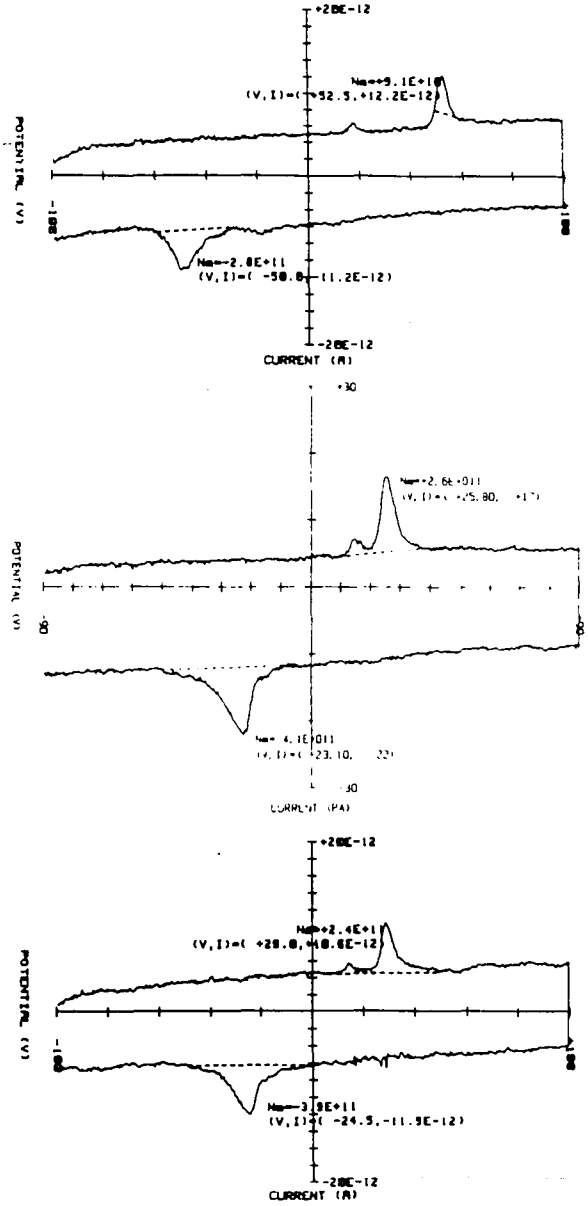

Figure 19. TVS Traces Obtained for Group 4.

The processing for group 5 simulates the resist etchback process used for the multilevel metal interconnect technology. Subgroup 5a in figure 20a has a sodium content of ≈ 8E13 cm^{-2}. Without any wet chemical cleans, the sodium level of the REB process is significant. With the addition of an EG/BHF wet chemical clean, as noted in subgroup 5b in figure 20b ,

the sodium level is reduced to ≈ 2E13 cm^{-2}. However, with the use of 100:1 HF, as shown in subgroup 5c in figure 20c, the sodium level detected is minimal.

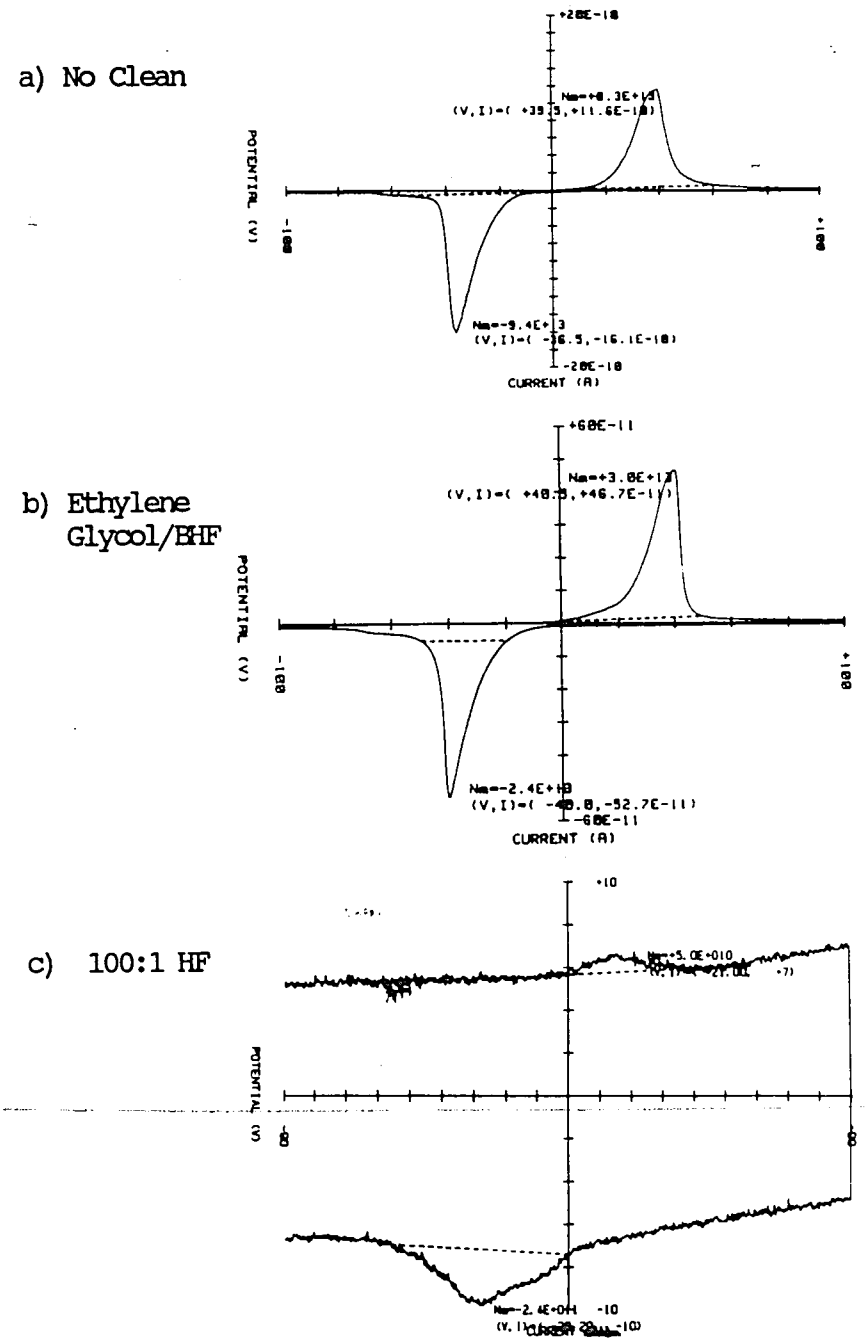

Figure 20. TVS Traces Obtained for Group 5.

Subgroup 3a (in figure 18a) has a high concentration of sodium and it will be used as an example to understand the TVS method of measuring the amount of sodium ions.

The silicon substrate is heated to 290 °C and is held at -100 volts for 180 seconds to attract all the sodium ions to the silicon-silicon dioxide interface. A linear ramp (0.5 volts per second) is started to initiate the movement of sodium ions to the silicon dioxide-metal interface under applied bias and elevated temperature. At +50 volts, the current begins to increase due to the movement of sodium ions. A peak is detected at +60 volts with the current stabilizing at ≈+80 volts. The voltage ramp continues to +100 volts and the substrate is held at this voltage for 180 seconds. The linear voltage is started in the reverse polarity and an increase in the current is detected at ≈-30 volts due to the movement of sodium ions. A peak is detected at ≈-40 volts with the current stabilizing at ≈-55 volts. The area under each curve is calculated and a concentration is obtained for each direction ($+N_m$, $-N_m$).

Comparing the sodium levels for subgroup 3a (≈ 8E11 cm^{-2}) with the levels obtained for subgroup 5a (≈ 8E13 cm^{-2}), it important to note the significant increase in sodium contamination due to the REB planarization process.

Initially, the study assumed that the sodium content would be higher using the REB planarization process, but it was never expected to be two orders of magnitude higher.

The oxide etch rate at room temperature of ethylene glycol/buffered hydrofluoric acid is ≈ 450 Å per minute and 100:1 hydrofluoric acid is ≈ 150 Å per minute. Therefore, the amount of oxide removed from all the subgroups receiving cleans should have been relatively equal. A dependence on etch chemistry is seen in this study along with detecting an increased level of sodium penetration into the dielectric when using the REB planarization process.

3.2 Incorporation of Phosphorus Doped Dielectric Two

It has been assumed that a high temperature (>800 °C) furnace step is necessary to getter sodium in a phosphorus doped dielectric. Here, the motivation was to study if a low temperature CVD dielectric doped with phosphorus could getter as effectively as a high temperature getter.

In the second experiment, group A acts as the control and insures that no sodium is present in the deposited film prior to any processing. Figure 21 shows the trace for group A.

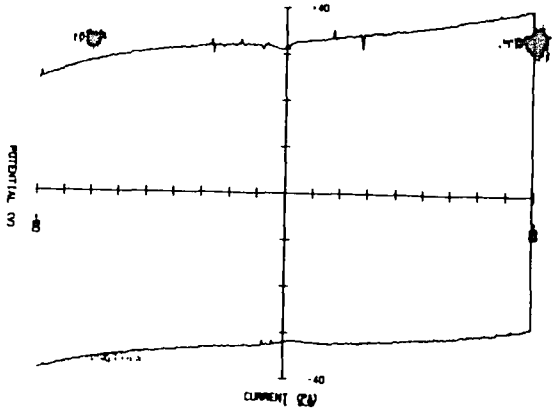

Figure 21. TVS Trace Obtained for Group A.

The TVS trace obtained for group B using the phosphorus doped PETEOS is similar to the trace for group A. The doped dielectric does not illustrate any unusual characteristics as is seen in figure 22.

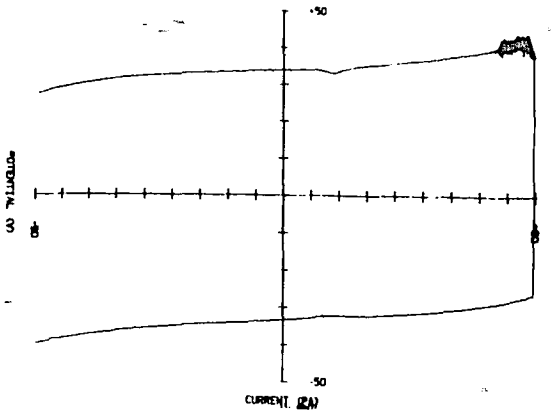

Figure 22. TVS Trace Obtained for Group B.

Wafers in group C were processed by depositing an undoped PETEOS layer, applying photoresist and oxygen plasma stripping the photoresist. These process steps were performed to guarantee sodium concentration and the levels of sodium detected were 8E11 cm^{-2}. This amount agrees with the concentrations obtained for subgroup 3a in the first experiment. Figure 23 shows the trace for group C.

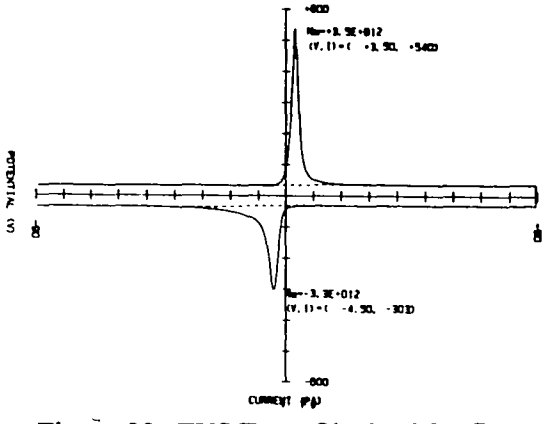

Figure 23. TVS Trace Obtained for Group C.

The results from group D are very impressive. With the same amount of sodium introduced into the phosphorus doped dielectric as was introduced in the undoped dielectric, the level of sodium detected is minimal. Figure 24 shows the trace for group D.

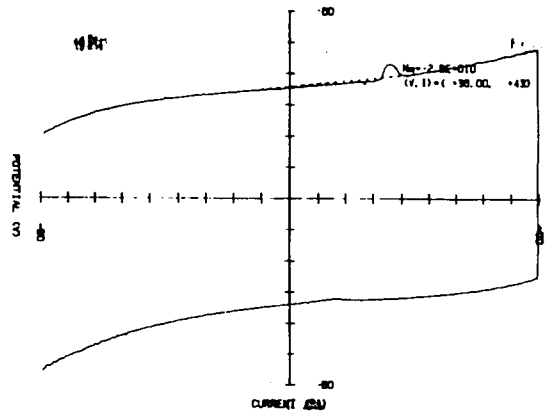

Figure 24. TVS Trace Obtained for Group D.

This suggests that the sodium has become trapped and therefore is inactive. The absence of a high temperature furnace step in this experiment suggests that a phosphorus doped plasma enhanced CVD dielectric using TEOS as the source gas may behave differently in its ability to trap sodium ions. Previous work reported has been on the mobility of sodium through thermally grown oxides or low temperature CVD oxides referenced in Section 2.1.

4. Summary and Conclusion

In integrated circuit processing, there are specific steps in the process that cause sodium contamination. Here, a dielectric process involving REB planarization developed for a multilevel metal interconnect technology is studied to determine its level of sodium contamination.

In this study, various etchback processes were evaluated for the amount of sodium contamination introduced during each process. In addition, post chemical cleans were evaluated for their effectiveness in removing the contaminated layer of dielectric prior to continued processing.

The triangular voltage sweep method was chosen to measure the sodium concentration for each dielectric process. Use of the TVS method provides pertinent information on the different mobile ion species present, as well as having the ability to detect densities as low as 10^9 cm^{-2}.

The results of the first experiment show that the REB planarization process introduces a higher sodium content than any of the other processes. The increase can be explained by the physical removal of the photoresist using an oxygen chemistry during the first etch step in the REB process. This provides an elevated level of sodium in the reactor which is driven deeper into the oxide during the subsequent etch steps in the REB etch recipe.

The post cleaning results showed that the 100:1 hydrofluoric acid is more effective in removing the contaminated layer of dielectric than the ethylene glycol/buffered etch.

As indicated by group 1 in the first experiment, ethylene glycol/buffered etch introduced a low level of sodium into an uncontaminated dielectric. Depending on the age of the bath, the level of sodium removed by the wet clean may be influenced by the amount of sodium already in the bath from previous wafers being cleaned.

In addition, this study included a second experiment that determined that a low temperature (<390 °C) phosphorus doped PETEOS dielectric was capable of gettering the sodium incorporated into the dielectric during oxygen plasma photoresist stripping. These results do not support the theory that a high temperature furnace step is necessary to getter the sodium.

Two of the main reasons that phosphorus was originally added to the dielectric was to getter sodium and to flow (or smooth) the dielectric. A dielectric containing phosphorus requires a high temperature (>800 °C) to flow the dielectric; however, a high temperature may not be necessary for gettering. Sodium is extremely mobile at low temperatures <400 °C (figure 25).[20] This mobility at low temperatures may explain the ability of the phosphorus doped dielectric to getter at a low temperature (390 °C) and a subsequent annealing step (<400 °C). Also, the process of depositing phosphorus doped PETEOS using a plasma enhanced CVD method may behave differently than the conventional CVD method.

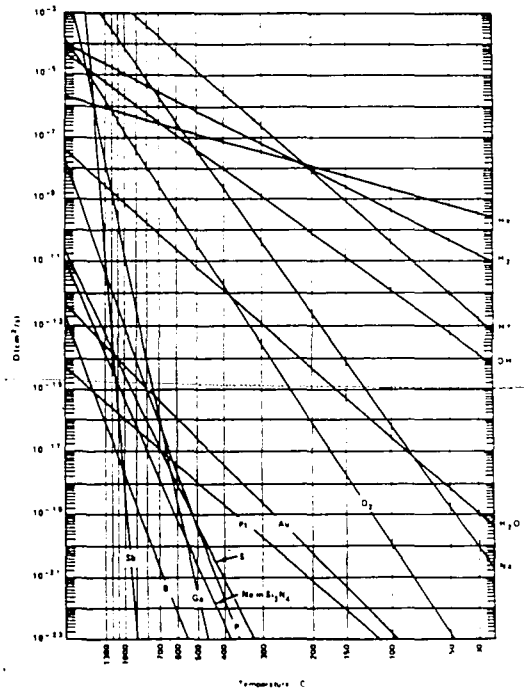

Figure 25. Diffusion Coefficient for Various Substances in SiO_2

In conclusion, introducing a new etch process as the REB planarization, into a multilevel metal interconnect technology, requires a complete evaluation of the process for sodium contamination. The suggested method for studying the process is by measuring the samples using triangular voltage sweep. Using this method, quantitative information on the amount of sodium contamination can be obtained and the specific step in the process sequence that is responsible for the contamination can be determined.

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